Single Event Effects Test Report for GSFC Test Trip to TAMU, 11 NOV 2003

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Introduction:
This testing was performed to determine the single event upset (SEU), single event functional interrupt (SEFI) and single event latchup (SEL) sensitivity of candidate devices for the Gamma Ray Large Area Space Telescope (GLAST) project. The devices tested were the GAFE (GLAST ACD Front End) ASIC, the GARC (GLAST ACD Readout Controller) ASIC, the MAX145 12-bit analog to digital converter (ADC), the MAX5121 12-bit digital to analog converter (DAC), and the MAX726 pulse width modulation DC/DC regulator. This testing was performed at the Texas A&M University Cyclotron.

Devices Tested:
The GAFE and the GARC are application specific integrated circuits (ASICs) that will be flown aboard GLAST in the Anti-Coincidence Detector (ACD) portion of the spacecraft. These devices are custom made and custom packaged. The die manufacturer is Agilent using their 0.5?m CMOS technology and the gate library chosen by the project. The devices were monitored by a custom test setup built by the ACD team at GSFC.

The MAX145 is a +2.7V, low power, 2-channel, 108ksps, serial 12-bit ADC, manufactured by Maxim Integrated Products. The complete part number for the MAX 145 is MAX145EUA, the lot date code is 0310, and the device markings are: 145 AFUA on the top and CIOA 0310 on the bottom.

The MAX5121 is a +3V/+5V, 12-bit, serial voltage-output DAC, with internal reference, manufactured by Maxim Integrated Products. The complete part number for the MAX5121 is MAX5121AEEE, the lot date code is 0134, and the device markings for the MAX5121 are: MAX5121 AEEE 134 on the top and NIPN 0134 on the bottom.

The MAX726 is a monolithic, bipolar, pulse width modulation (PWM), switch-mode DC/DC regulators optimized for step-down applications, rated for 2A and was manufactured by Maxim Integrated Products. This device was monitored for SEL only. The devices were marked MAXIM MAX726ECK 0317RI.

Test Facility Information:
The devices were tested at the Texas A&M University Cyclotron Facility (TAMU). The cyclotron was tuned to 15MeV/amu for the beams used in testing. A complete list of beams and relevant information is given below. The LET values may vary slightly due to a difference in distance from the device to the beam window. All devices were mounted in air at the end of the Radiation Effects Facility line off of the K500 cyclotron.

Ion	Angle of Incidence	LET or LET_{eff} ($MeV \cdot cm^2/mg$)	Range in Silicon (?m)
Neon	0	2.69	281
Argon	0, 45, 60	8.7, 12.3, 17.4	194, 131, 93
Copper	0	19.5	137
Krypton	0, 45, 60	27.7, 40.2, 56.8	127, 90, 63
Xenon	0, 45	51.3, 75.9	121, 72

Test Setups:
The GAFE Heavy Ion Test Setup consisted of two printed circuit boards (PCBs), power supply, control computer, and digital multimeters. One of the PCBs contained Device Under Test (DUT) and the other PCB was an auxiliary board which received commands from control computer via serial communication, exercised DUT, collected data and sent them back to the control computer. The controller then compared data to the preset values to determine the

occurrence of error(s). GPIB controlled digital multimeters monitored supply current to DUT while it was irradiated. Figure below depicts this setup.

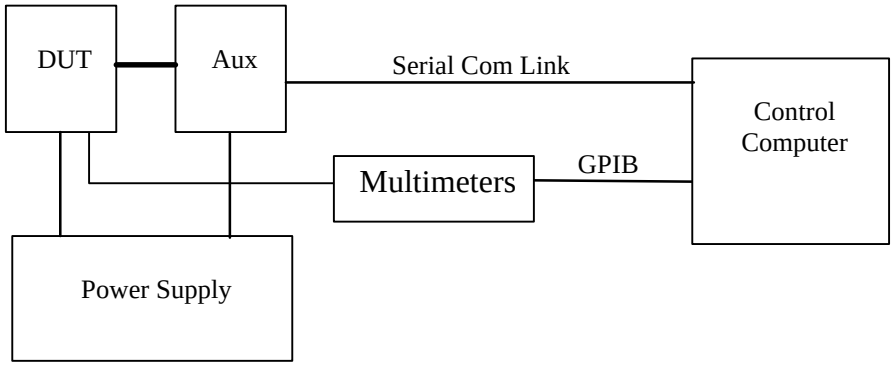


Figure 1: GAFE Heavy Ion Test Setup

Two PCBs with interconnecting cable and power supply as well as software to control them and capture errors were provided by the GLAST project. The control computer and multimeters with the program to monitor the current were provided by the Radiation Effects Analysis Group, Code 561.

GARC Heavy Ion Test Setup consisted of two printed circuit boards (PCBs), power supply, control computer, and digital multimeter. One of the PCBs contained Device Under Test (DUT) and the other PCB was an auxiliary board which received commands from control computer via serial communication, exercised DUT, collected data and sent them back to the control computer. The controller then compared data to the preset values to determine the occurrence of error(s). GPIB controlled digital multimeter monitored supply current to DUT while it was irradiated. Figure below depic p.

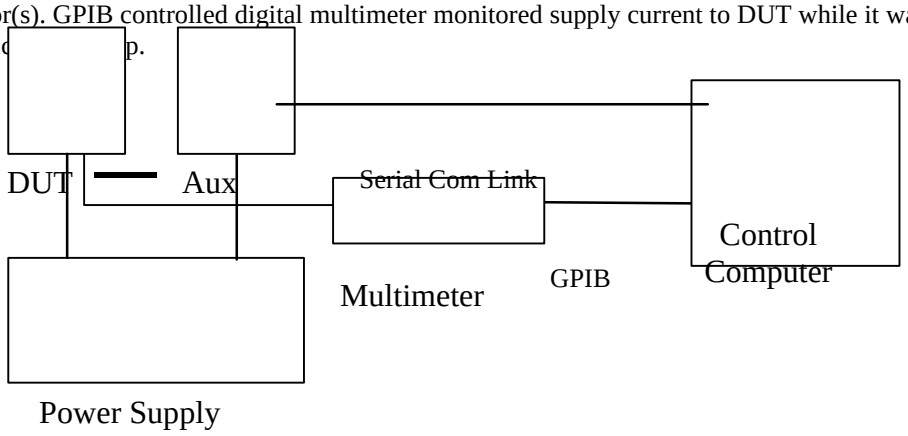


Figure 2: GARC Heavy Ion Test

Two PCBs with interconnecting cable and power supply as well as software to control them and capture errors were provided by the GLAST project. The control computer and multimeter with the program to monitor the current were provided by the Radiation Effects Analysis Group, Code 561.

For the ASICs, the signals for SET and SEFI were picked off the test board by the custom LABVIEW test software provided by the project (ACD group). The software broke down the captured errors into data columns 1, 2 and 3. Errors are reported by column and by total number. The devices were monitored for SEL across a resistor on the test board (device current). It should be noted that due to the design of the sockets used to hold the ASICs, no angle of incidence data could be taken. It should also be noted that not all of the sections of each ASIC could be tested for

SET/SEFI/SEL with the software configured as it was for this test. For the GAFE, only the digital command logic registers were tested. For the GARC, the portions of the ASIC "visible" to the test set were: LVDS receivers for the "A" side of the device, the look-at-me and reset logic, the portion of the command and trigger processor containing the logic registers, a portion of the event data formatter, and the a portion of the LVDS drivers.

The MAX5121 D/A and MAX145 A/D converters were tested by providing the correct input signal to the D/A and then feeding its output to the A/D. The digital output from the A/D is then monitored for changes by using external circuitry. The D/A and A/D converters were operated at a conversion rate of about 20kHz and a clock pulse rate of 1MHz. The basic block diagram for the design is on Figure 3.

The D/A MAX5121 was configured to simultaneously load input and DAC registers by sending control bits of 010. After the control bits, the data bits are sent then a sub-bit, which is always zero. The SCLK and the CS\ signals were generated using a programmable chip (PAL22V10B). The PAL22V10 also generated a clock signal called SDCLK for the shift registers that were used to provide the DIN for the MAX5121. Proper methodologies were used in order to make sure the timing requirements for the D/A were met. The DIN signal for the D/A is configurable by flipping dipswitches; this allows the output of the D/A to be varied. Figure 4 shows how the D/A input and output pins were connected.

Using the same SCLK and CS\ signals configured the A/D MAX145 for proper operation. Proper methodologies were used in order to make sure the timing requirements for the A/D were met. The analog input signal needed by the A/D came from the D/A and the reference voltage from a 2.5V voltage ref (MAX6325). The output of the A/D was checked in order to make sure it concurs with the input. The D/A and A/D configuration, timing and setup were determined to be functioning correctly at the lab and at the test facility. All Devices Under Test (DUT) were measured and verified for functionality before each test. Figure 4 shows how the A/D inputs and outputs were connected.

The method decided upon in order to test the D/A and A/D setup for errors is to compare the output of the A/D with a reference signal. This is accomplished by using shift registers to generate a copy of the A/D output. Dipswitches are used to vary the output of the reference signal. After the reference signal was matched with the A/D output, the two signals are then fed in a XOR gate. The output of the XOR gate is then fed into a flip-flop (74LS74) to ensure the timing glitch cause by the two signals being fed in the XOR gate is fixed.

Since the D/A and A/D test board was constructed using a wirewrap board, resolution of the A/D output is not stable on the last 2 LSB's. This problem was fixed by using a PAL22V10 to mask the bits. The PAL22V10 LSB mask chip is capable of masking the last 4 LSB's by toggling dipswitches. The output of this mask chip is then connected to the reset pin of the flip-flop. The output of the flip-flop is then fed into an edge-triggered counter. This allows the test engineer to see and count the errors being induced by the radiation effects in real time.

In order to reduce noise on the test board, the D/A and the A/D were mounted on a copper board with all traces etched and all capacitors used were surface mount. This copper board or test socket can then be removed and swapped with other test sockets on the wirewrap board. Since the D/A and the A/D were mounted in close proximity and on the same test socket, the device not being test during irradiation is covered with sufficiently thick material to protect it from the heavy ions.

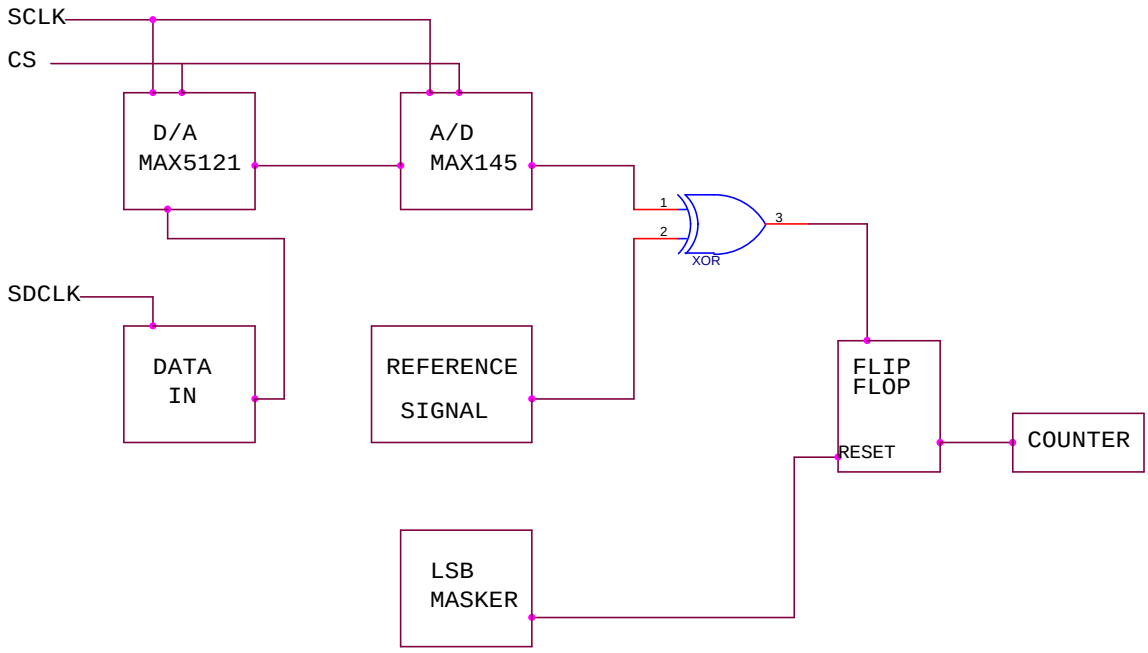


Figure 3: Basic Block Diagram for MAX5121 and MAX145 test board.

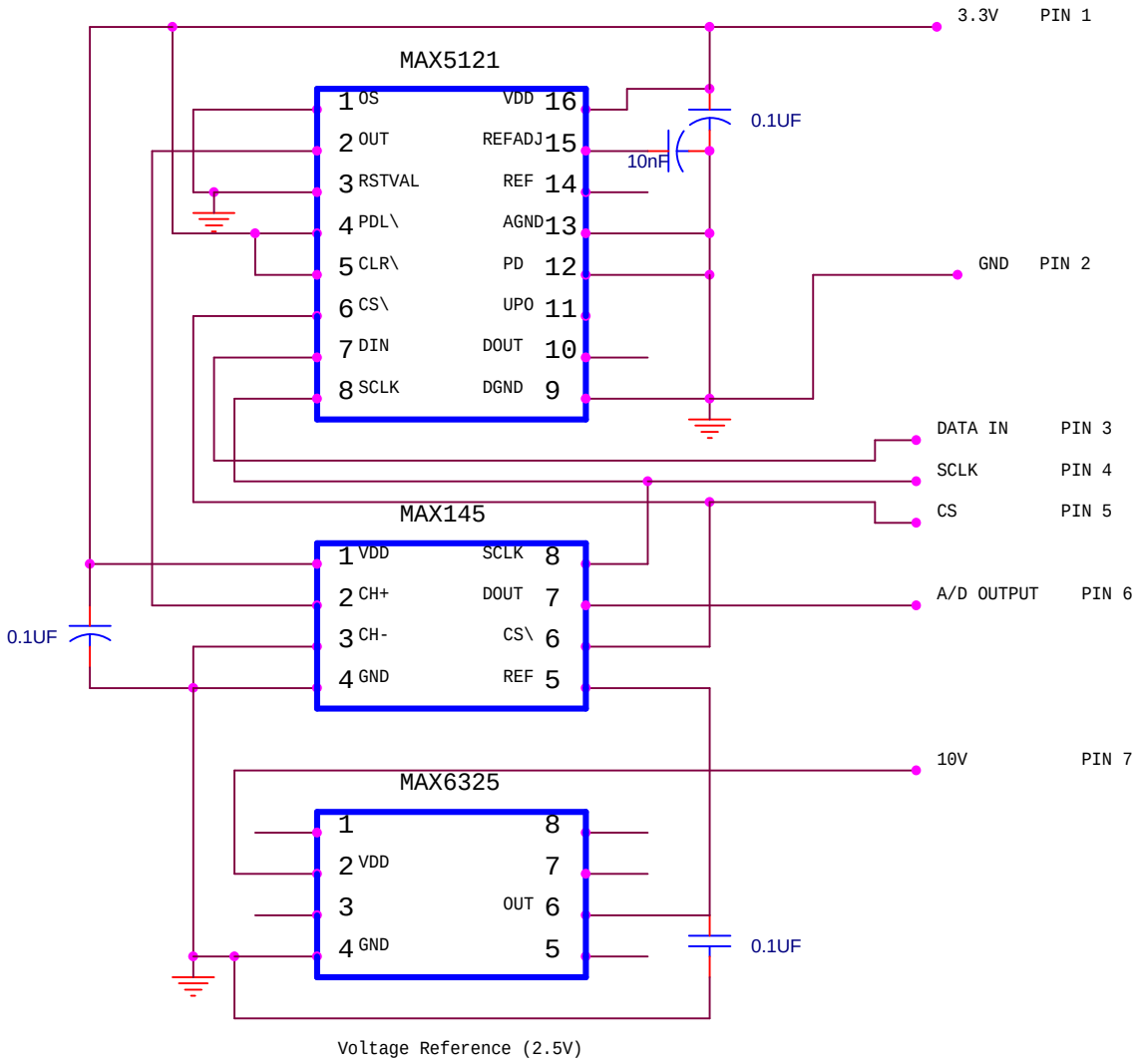


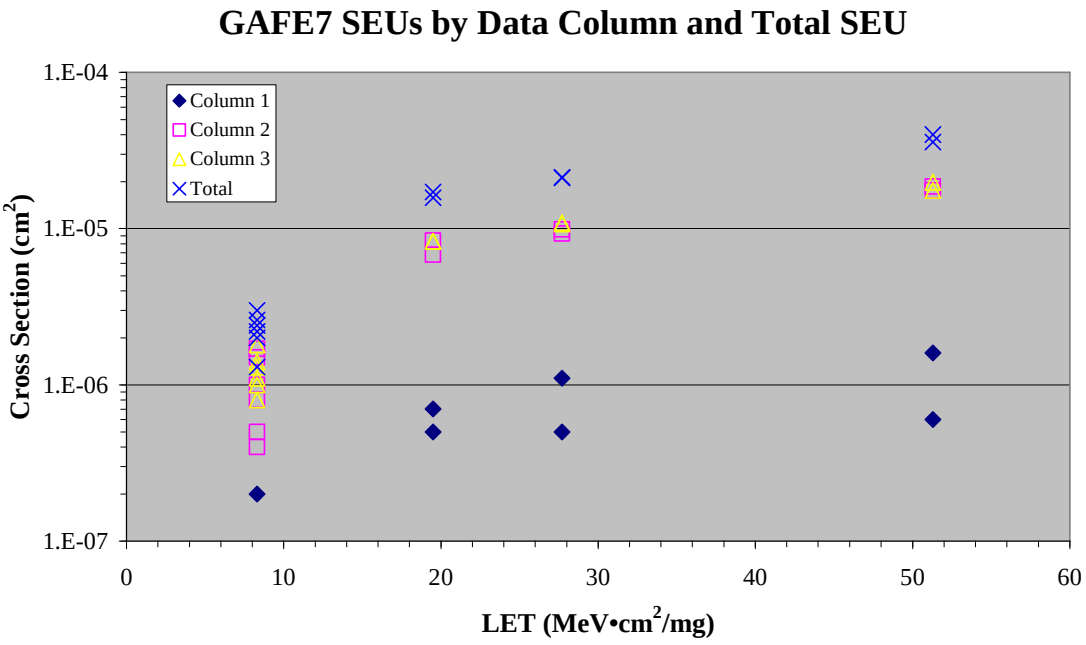
Figure 4: Pin configurations for the MAX5121 and MAX145.

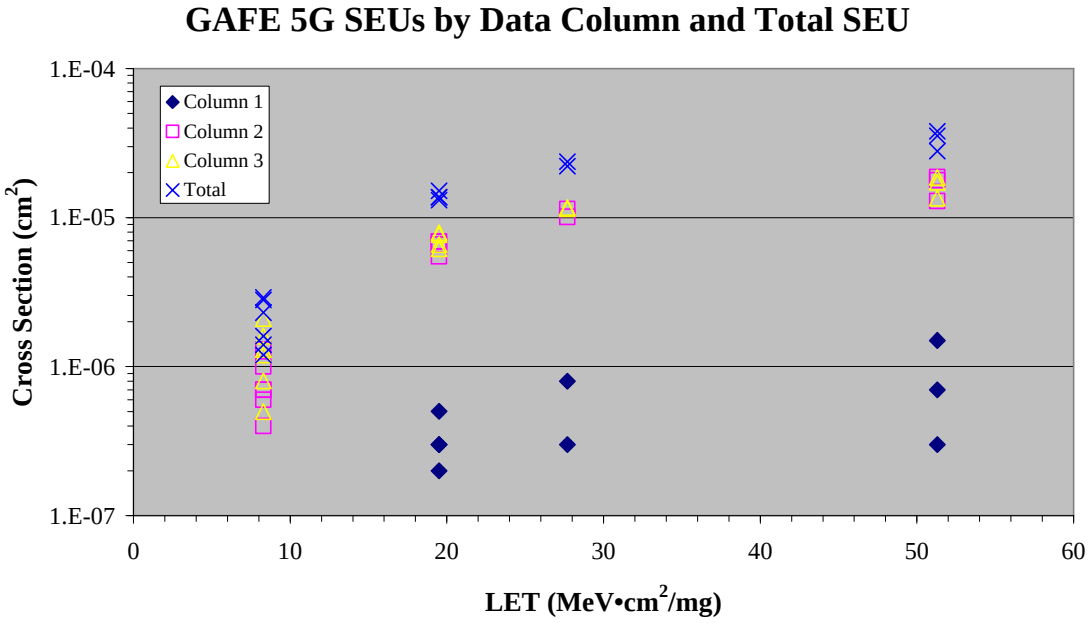
The MAX145 ADC and MAX5121 DAC were monitored for SET and SEFI. The devices were powered by an HP6654A quad DC power supply. The output of the devices was monitored by a custom test program written in LABVIEW, all of the equipment and the devices were controlled by this program through a GPIB interface. The three-page test board schematic is given as an appendix to this report.

The MAX726 PWM DC/DC regulator was monitored for SEL only. This was a continuation of the previous SEL testing done at TAMU. This test was specifically for the MAX726 flight lot. The test boards used were custom evaluation boards made by the SLAC group powered by an HP6654A quad DC power supply. The output current was monitored for latchup.

Results:

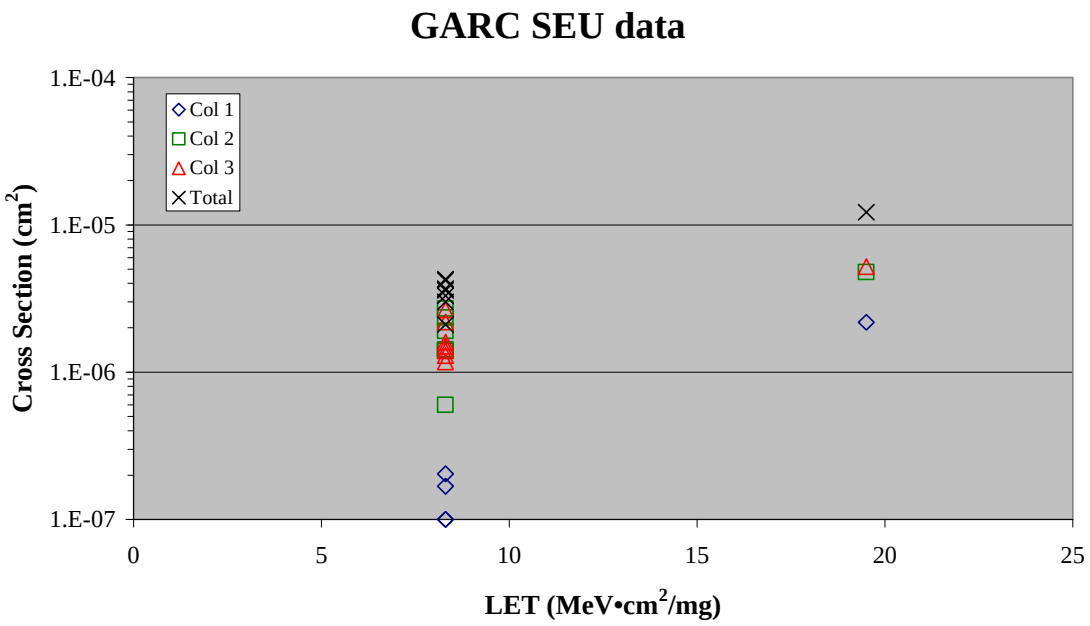
Two each of the GAFE7 and GAFE5G were irradiated to determine the SEU, SEFI and SEL sensitivity of the devices. None of the 4 devices exhibited SEL to a fluence of $1x10^{7}$ ions/cm^2 of Xe with an LET of 51.3 MeV•cm^2/mg (Xe at normal incidence) and there was no indication of a SEFI during any run. The limiting cross section is therefore less than $1.0x10^{-7}$ cm^2 per device for SEL and SEFI. Both versions of the GAFE were sensitive to SEU. The threshold for both versions is given by 2.7 MeV•cm^2/mg $<LET_{TH}$ < 8.3 MeV•cm^2/mg. The limiting cross section is ~$4x10^{-5}$ cm^2/device. Graphs of the cross section data are given below. The rates for both versions were sufficiently similar that the rate predictions are the same for both. The predicted SEU error rate from CREME96 is $9.52x10^{-5}$ SEU/device/day.

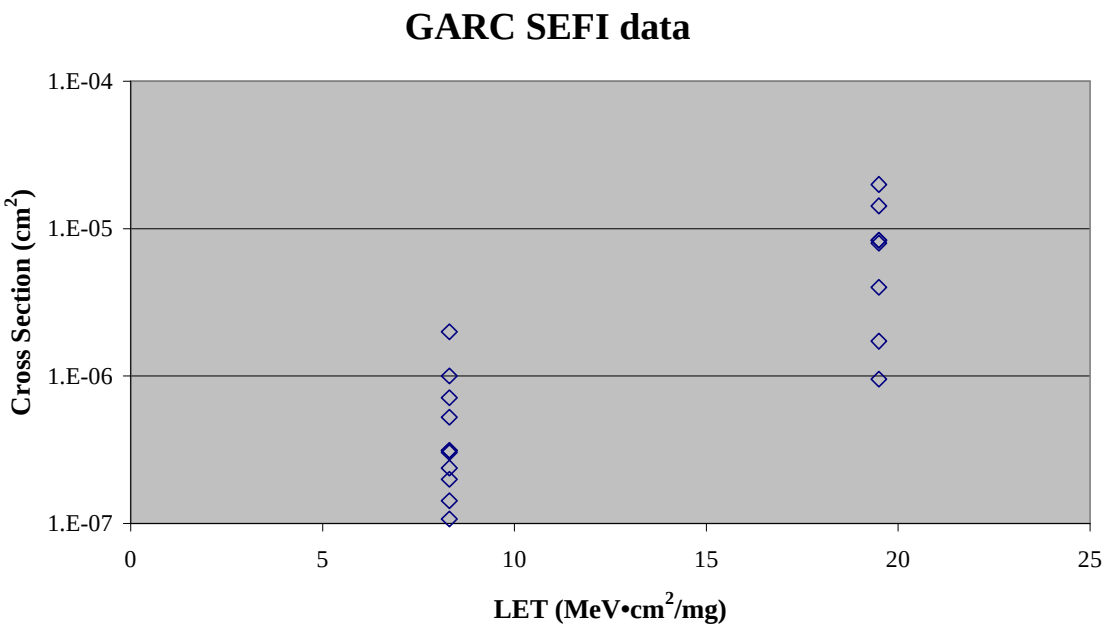




Two GARC devices were irradiated to determine their SEU, SEFI and SEL sensitivity. The rate of the SEFI events overwhelmed the testing of the devices and rendered SEL screening to an appropriate level impossible. The SET data is also severely hampered by this SEFI. The data obtained is statistically less than ideal for accurate rate prediction. The threshold for both SET and SEFI is given by 2.7 MeV•cm^2/mg <LET_{TH} < 8.3 MeV•cm^2/mg. The limiting cross section is predicted to be ~1x10^{-4} cm^2/device. Graphs of the cross section data are given below. Given the limited data, the rate for SEU will be assumed to be equivalent to the rate for SEFI. The predicted SEU

error rate from CREME96 is $2.74x10^{-4}$ SEU/device/day. The predicted SEFI error rate from CREME96 is $2.74x10^{-4}$ SEFI/device/day.

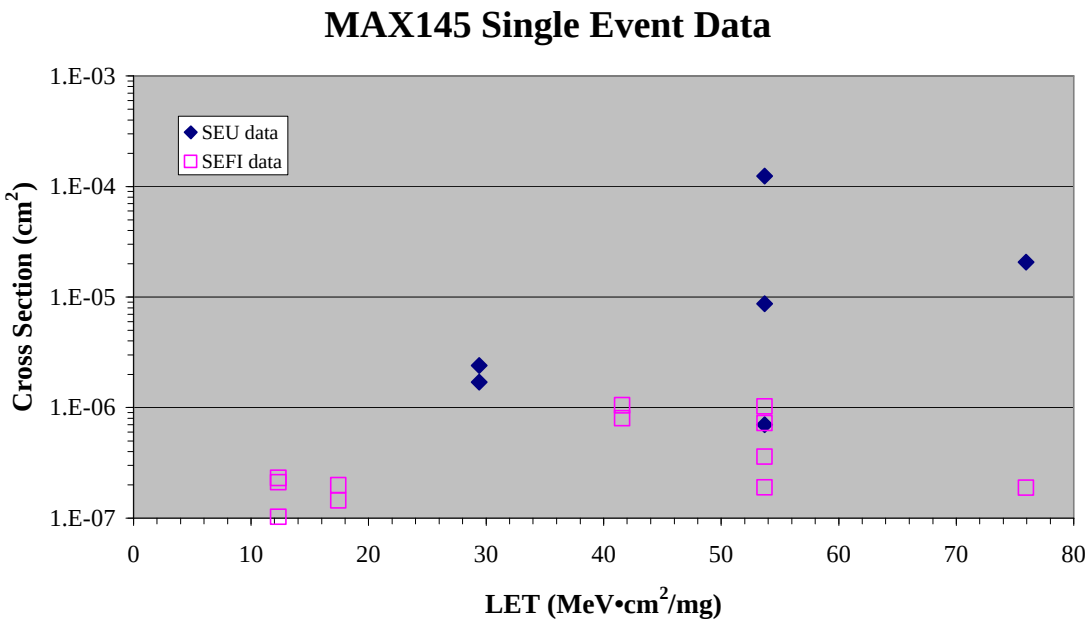




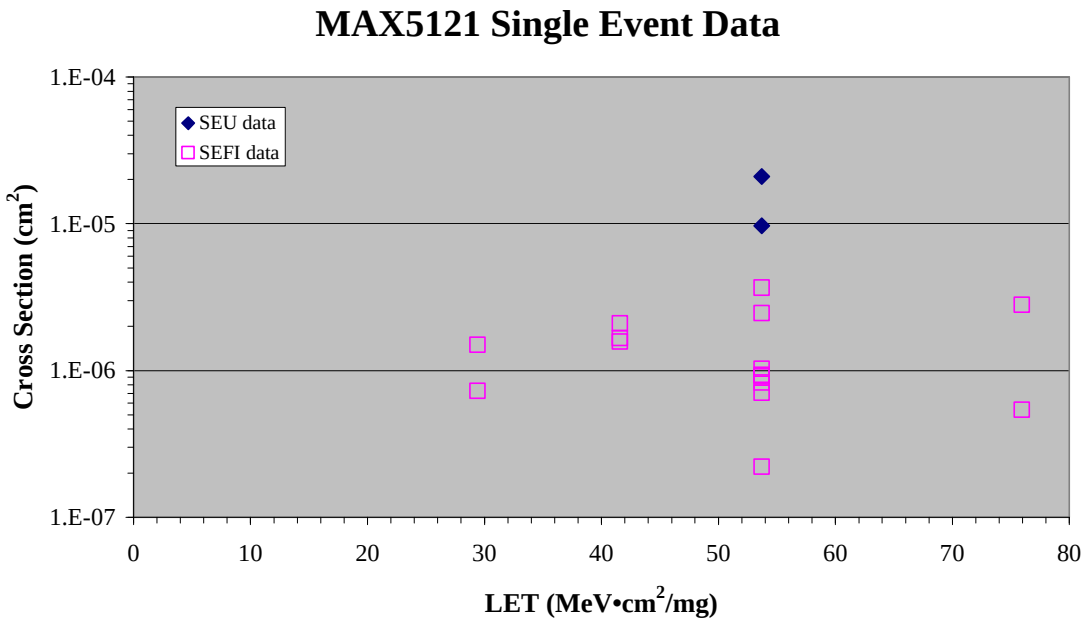
Four MAX145 ADCs and three MAX5121 DACs were irradiated to determine the SEU, SEFI and SEL sensitivity of the devices. Two devices of each type were irradiated with $3x10^{8}$ions/cm^2 of the highest LET ion used. Neither the MAX145 nor the MAX5121 exhibited SEL to an LET of 53.9 MeV•cm^2/mg (Xe at normal incidence). The cross section is less than $3.33x10^{-9}$ cm^2 per device for both converters.

The MAX145 was sensitive to SEU and SEFI. For SEU, the threshold is predicted to be ~17 MeV•cm^2/mg. The limiting cross section is predicted to be ~$2.8x10^{-5}$ cm^2/device. The predicted SEU error rate from CREME96 is

1.25x10^{-6} SEU/device/day. For SEFI, the threshold is predicted to be ~10 MeV•cm^2/mg. The limiting cross section is predicted to be ~1.1x10^{-6} cm^2/device. The predicted SEFI error rate from CREME96 is 3.54x10^{-8} SEFI/device/day.



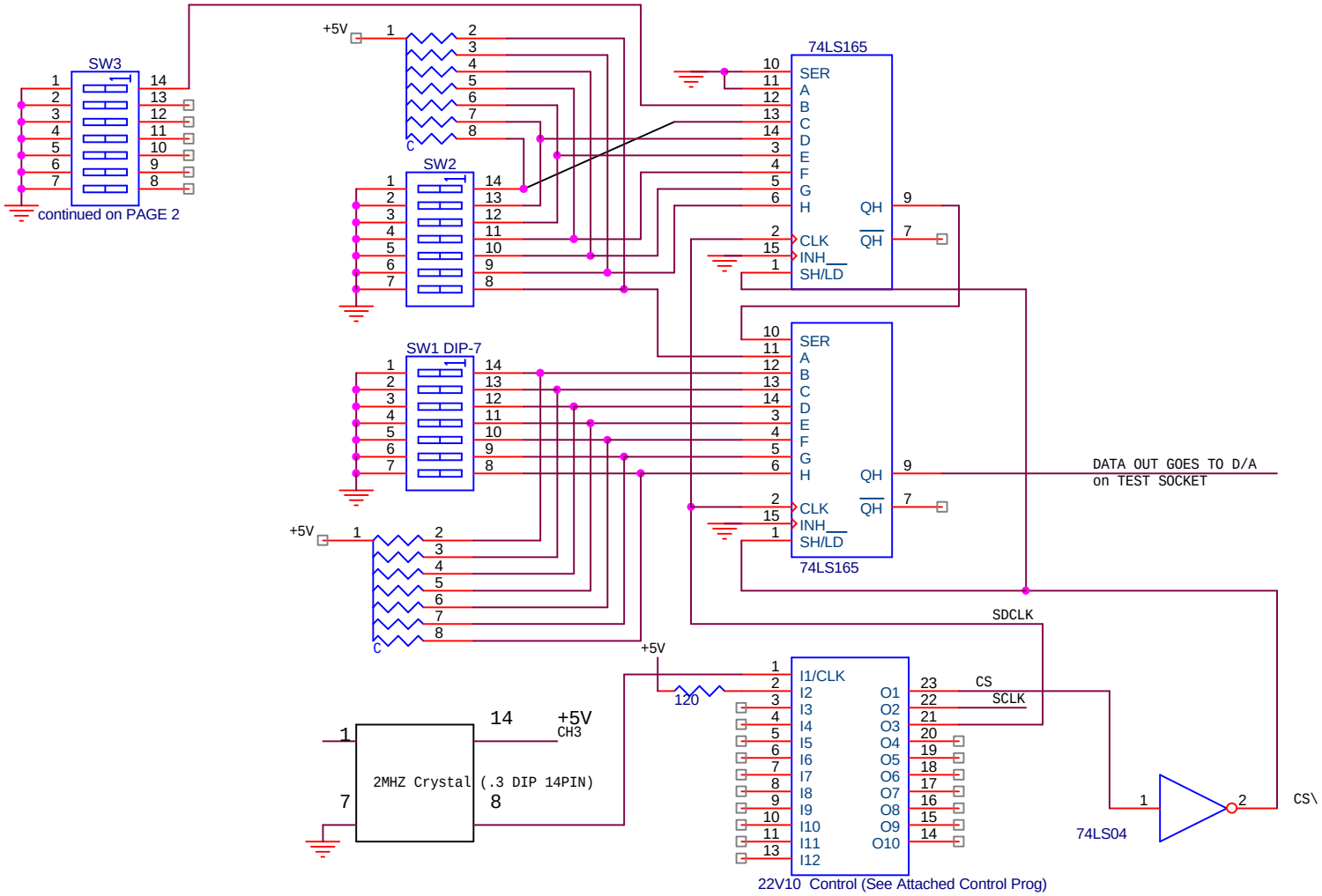
The MAX5121 was sensitive to SEU and SEFI. For SEU, the threshold is predicted to be ~18 MeV•cm^2/mg. The limiting cross section is ~8x10^{-4} cm^2/device. The predicted SEU error rate from CREME96 is 1.23x10^{-4} SEU/device/day. For SEFI, the threshold is predicted to be ~18 MeV•cm^2/mg. The limiting cross section is ~4x10^{-6} cm^2/device. The predicted SEFI error rate from CREME96 is 5.19x10^{-8} SEFI/device/day.



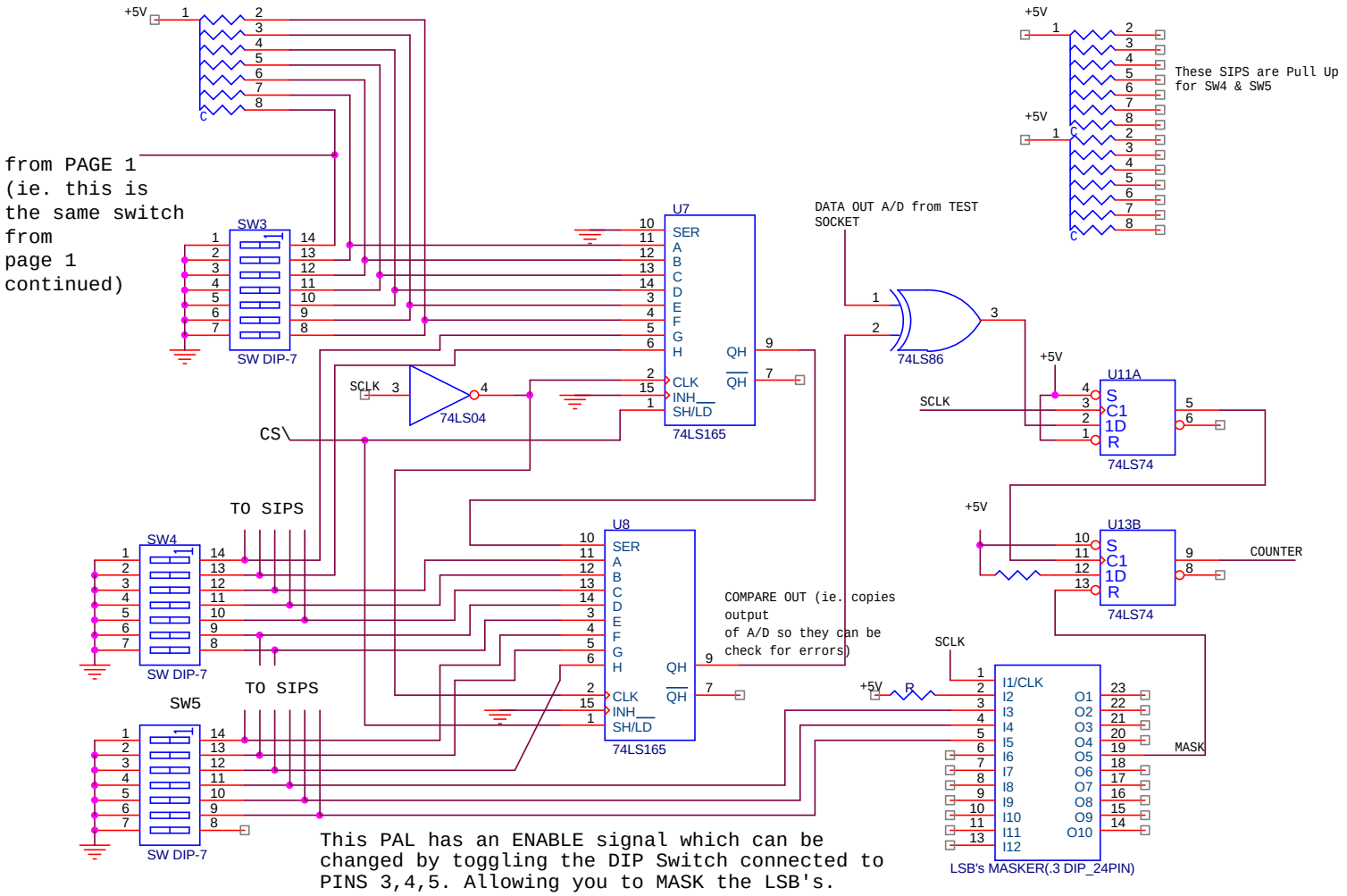
The three MAX726 DC/DC regulators showed no latchup during testing. The devices did show significant thermal issues and in each case, the test was stopped for a thermal failure of the device. It should be noted that the evaluation board did not have sufficient heatsink mass to properly cool the device. This should be taken into account in device placement and usage. The devices were tested at 0? (LET = 53.7MeV•cm^2/mg) and 45? (LET$_{eff}$ = 75.9 MeV•cm^2/mg) with Xe. The limiting cross-section for SEL is less than 1x10^{-8}cm^2 for both conditions given.

The following three pages contain the schematic for the ADC and DAC radiation effects test board.

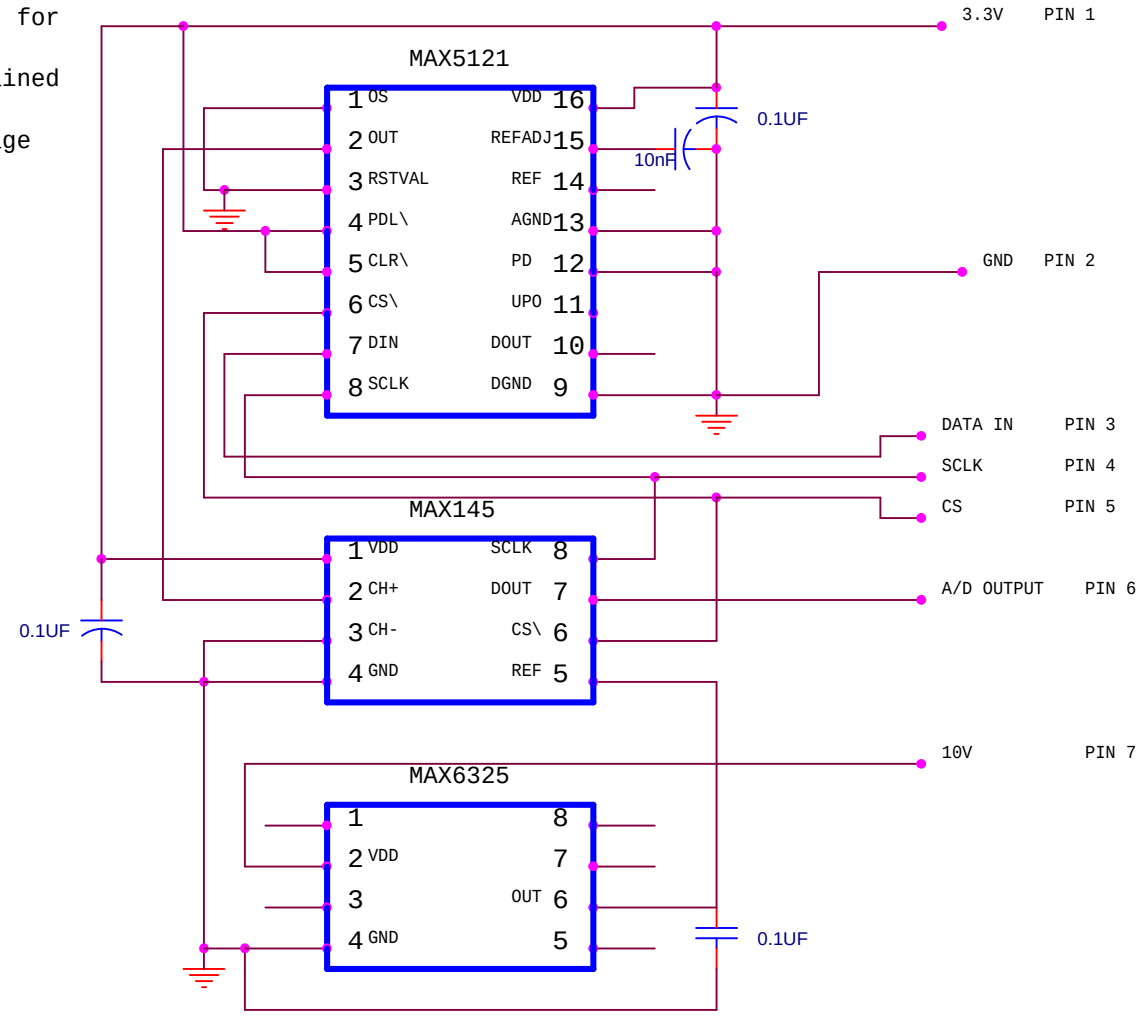
PAGE 1



PAGE 2


from PAGE 1
(ie. this is
the same switch
from
page 1
continued)
+5V
SW3
SW DIP-7
U7
SER
A
B
C
D
E
F
G
H
CLK
INH
SH/LD
QH
74LS165
SCLK
74LS04
CS\
DATA OUT A/D from TEST
SOCKET
74LS86
U11A
S
C1
1D
R
74LS74
These SIPS are Pull Up
for SW4 & SW5
TO SIPS
SW4
SW5
SW DIP-7
U8
COMPARE OUT (ie. copies
output
of A/D so they can be
check for errors)
U13B
COUNTER
MASK
I1/CLK
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I12
O1
O2
O3
O4
O5
O6
O7
O8
O9
O10
LSB's MASKER(.3 DIP_24PIN)
This PAL has an ENABLE signal which can be
changed by toggling the DIP Switch connected to
PINS 3,4,5. Allowing you to MASK the LSB's.

This is the test socket for the parts.
-the test sockets contained both the D/A
and the A/D and a Voltage Ref



Voltage Reference (2.5V)